60V N-Channel Enhancement Mode MOSFET

■ DESCRIPTION

The SL2308 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.
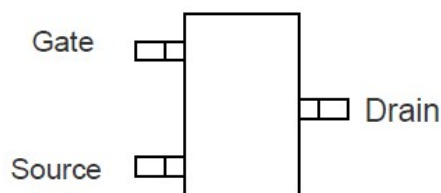
■ FEATURE

◆ *60V/1. 8 A, $R_{DS(ON)}$=135mΩ(typ.)@VGS=10V*

◆ *60V/ 1.5 A, $R_{DS(ON)}$=154mΩ (typ.)@VGS=4.5V*

◆ Super high design for extremely low $R_{DS(ON)}$

◆ Exceptional on-resistance and Maximum DC current capability

◆ This is a Full RoHS compliance

◆ SOT23-3 package design

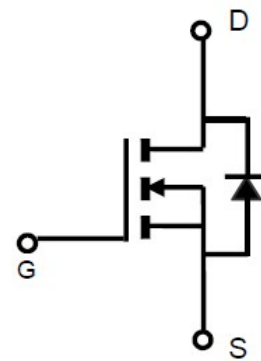## ■ APPLICATIONS

◆ Power Management in Note Book

◆ Portable Equipment

◆ Battery Powered System

■ PIN CONFIGURATION

TOP VIEW
SOT-23

N-Channel

■ *ABSOLUTE MAXIMUM RATINGS* (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current (TJ=150℃)	VGS-4.5V	1.8	A
I_{DM}	Pulsed Drain Current		10	A
I_S	Continuous Source Current (Diode Conduction)		1	A
P_D	Power Dissipation	TA=25℃	1.25	W
		TA=75℃	0.8	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *THERMAL DATA*

Symbol	Parameter	Min	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		62.5	125	℃/W

ELECTRICAL CHARACTERISTICS(VDD=2.75V, T_A=25℃ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.0		2	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=44V, V_{GS}=0			1	uA
		V_{DS}=44V, V_{GS}=0 T_J=85℃			5	
$I_{D(ON)}$	On=State Drain Current	V_{DS}≥5V, V_{GS}=4.5V	10			A
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS} =10V,I_D=1.8A		135	160	mΩ
		V_{GS}=4.5V, I_D=1.5A		154	200	
G_{fs}	Forward Transconductance	V_{DS}=5V, I_D=2.1A		10		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=1.0A, V_{GS}=0V		0.8	1.0	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=27V		2.1	3.9	nC
Q_{gs}	Gate-Source Charge	V_{GS}=4.5V		0.6		
Q_{gd}	Gate-Drain Charge	I_D=2.1A		0.8		
C_{iss}	Input Capacitance	V_{DS}=25V		295		pF
C_{oss}	Output Capacitance	V_{GS}=0V		40		
C_{rss}	Reverse Transfer Capacitance	f=1MHz		15		
$T_{d(on)}$	Turn-On Time	V_{DS}=27V		3.6		nS
T_r		R_L=10Ω		3.5		
$T_{d(off)}$	Turn-Off Time	I_D=1A		32		
T_f		V_{GEN}=4.5V R_G=6Ω		3		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2.Static parameters are based on package level with recommended wire bonding

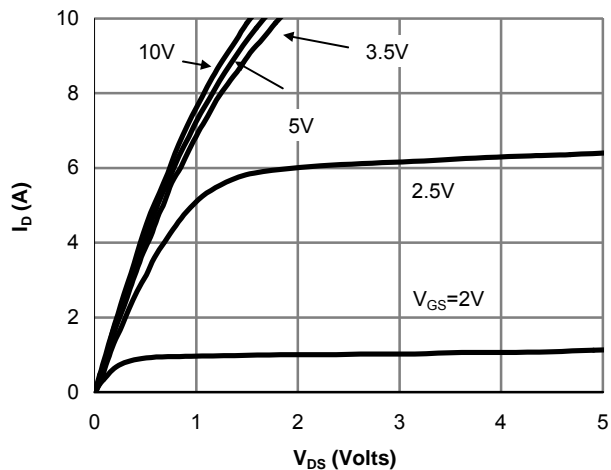■ *TYPICAL CHARACTERISTICS (25℃   Unless Note)*
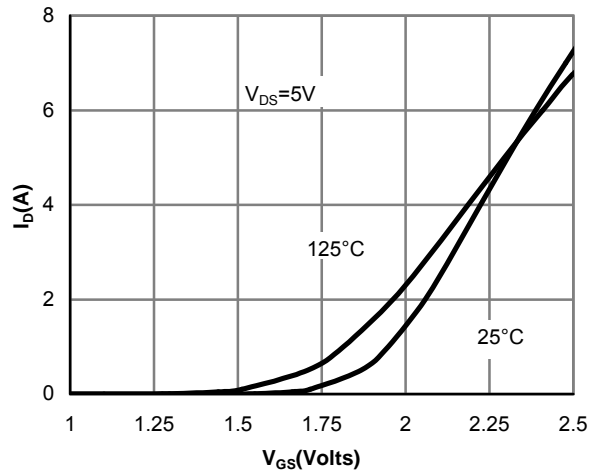
Fig 1: On-Region characteristics

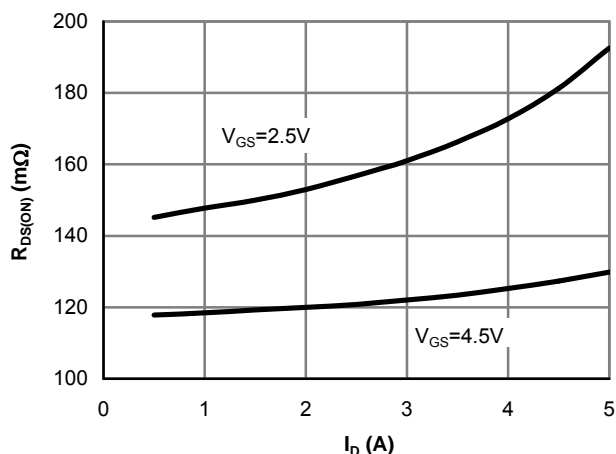**Figure 2: Transfer Characteristics**

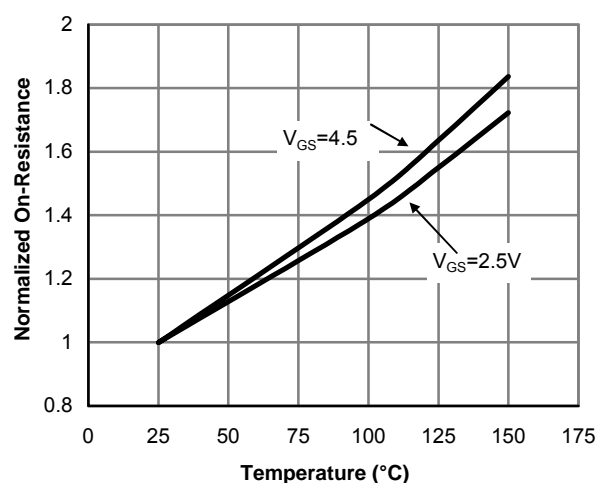**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**

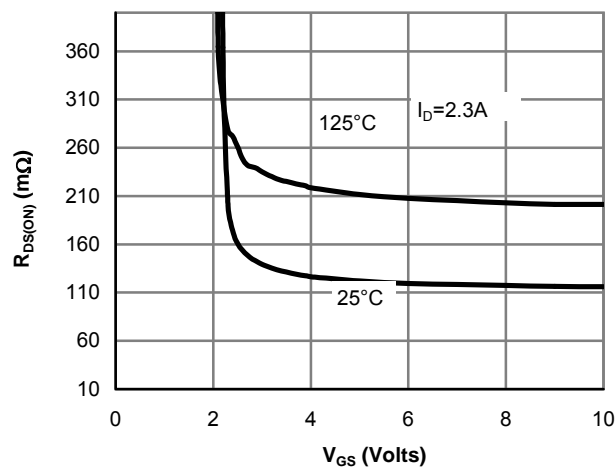**Figure 4: On-Resistance vs. Junction Temperature**
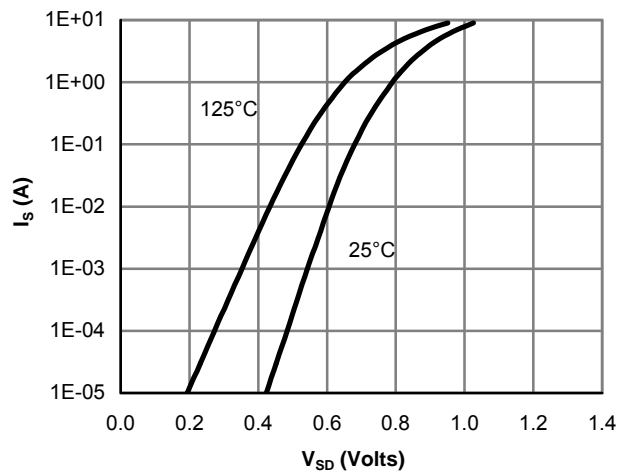
Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics

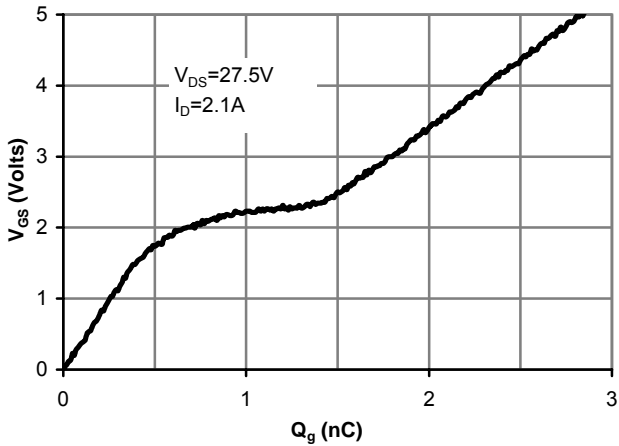■ *TYPICAL CHARACTERISTICS (continuous)*
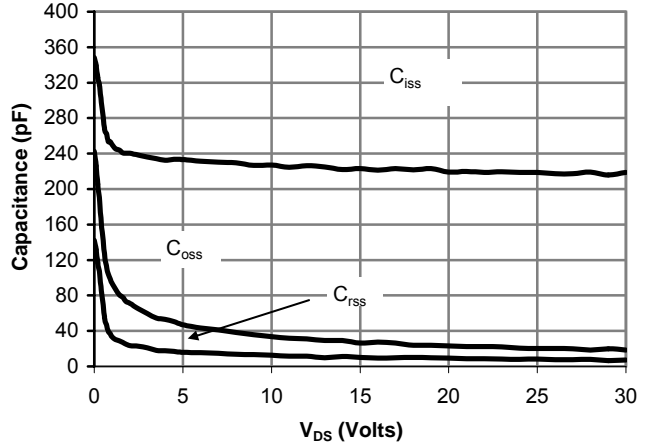
Figure 7: Gate-Charge Characteristics
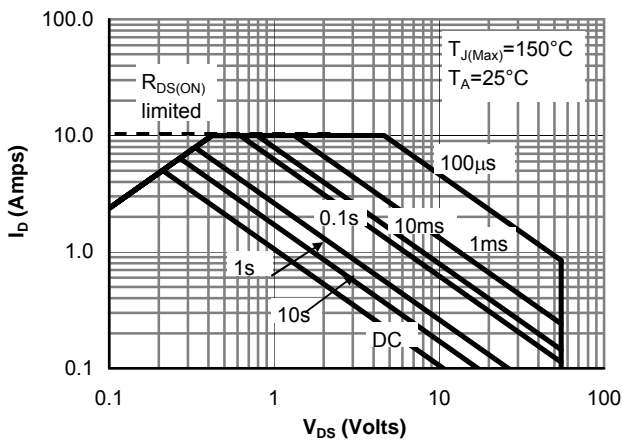
Figure 8: Capacitance Characteristics

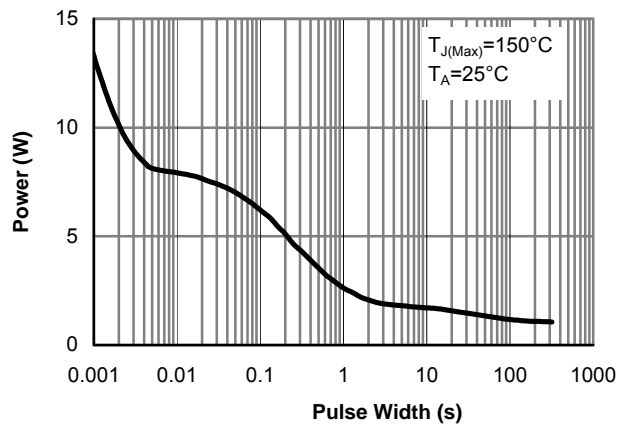Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

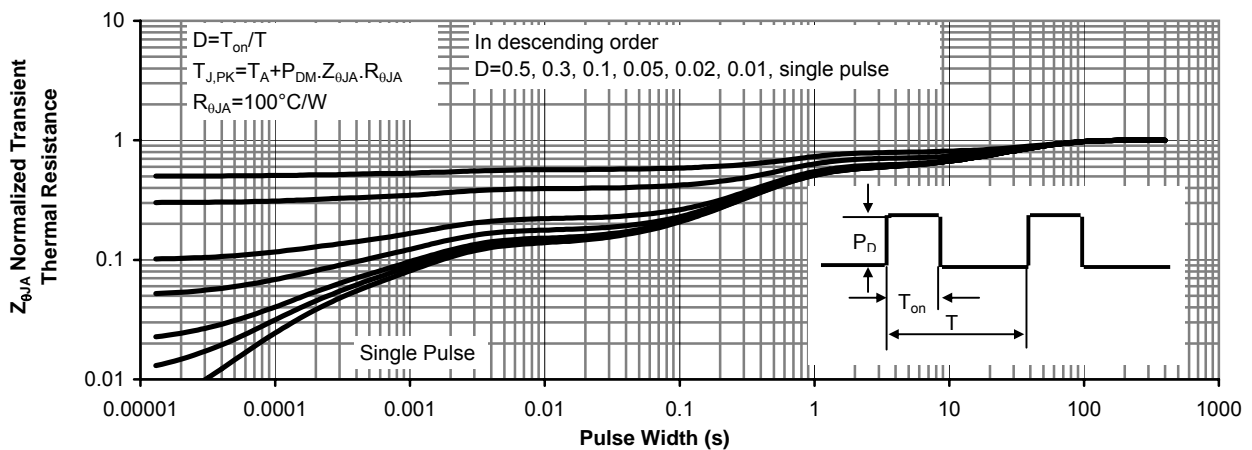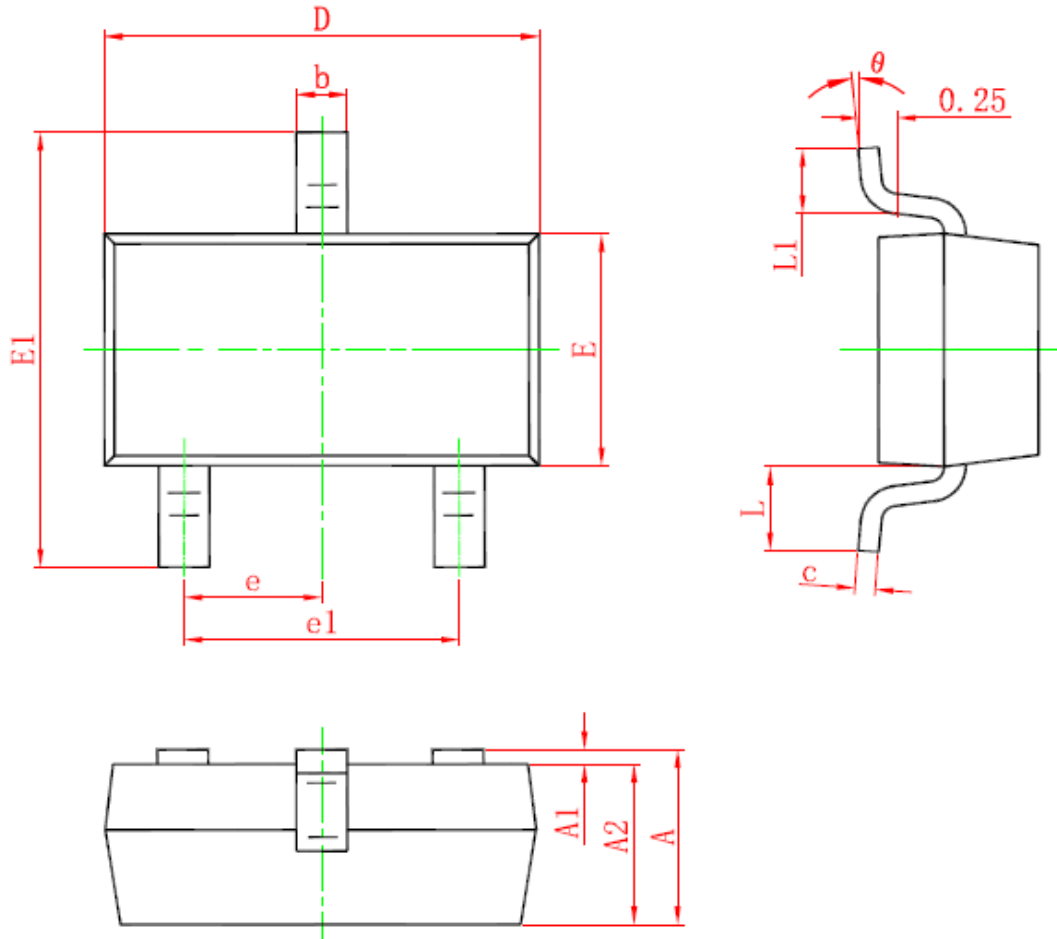Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

Figure 11: Normalized Maximum Transient Thermal Impedance

■ *SOT23 PACKAGE OUTLINE DIMENSIONS*

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°